



PTO/SB/08A (08-03)

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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Complete if Known

Application Number	10/803,273
Filing Date	March 18, 2004
First Named Inventor	Richard W. Foote
Art Unit	2812 2823
Examiner Name	Not Yet Assigned Foursa
Attorney Docket Number	P05827

Sheet 1 of 2

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
(F)	AA	US- 4,631,803	12/30/1986	Hunter et al.	
(F)	AB	US- 4,835,115	05/30/1989	Eklund	
(F)	AC	US- 4,983,226	01/08/1991	Hunter et al.	
(F)	AD	US- 5,106,777	04/21/1992	Rodder	
(F)	AE	US- 5,358,891	10/25/1994	Tsang et al.	
(F)	AF	US- 5,448,102	09/05/1995	Gaul et al.	
(F)	AG	US- 5,468,676	11/21/1995	Madan	
(F)	AH	US- 5,474,953	12/12/1995	Shimizu et al.	
(F)	AI	US- 5,683,908	11/04/1997	Miyashita et al.	
(F)	AJ	US- 5,872,044	02/16/1999	Hemmenway et al.	
(F)	AK	US- 5,874,317	02/23/1999	Stolmeijer	
(F)	AL	US- 5,920,108	07/06/1999	Hemmenway et al.	
(F)	AM	US- 6,069,057	05/30/2000	Wu	
		US-			
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				

Examiner Signature	Foursa	Date Considered	8/19/05
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Sheet 2 of 2

Application Number	10/803,273
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First Named Inventor	Richard W. Foote
Art Unit	2842 2823
Examiner Name	Not Yet Assigned <i>Fourson</i>
Attorney Docket Number	P05827

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
G	BA	Naresh Thapar et al., "Elimination of the "Birds Beak" in Trench MOS-Gate Power Semiconductor Devices", Power Semiconductor Research Center, 1996 IEEE, Pp. 83-86.	
G	BB	G. Fallico et al., "A New Process for Defect-Free Definition of Active Areas in Deep Trench Isolated Bipolar Devices", Microelectronic Engineering 15 (1991) Pp. 655-658.	
G	BC	R. Bashir et al., "PLATOP: A Novel Planarized Trench Isolation and Field Oxide Formation Using Poly-Silicon", IEEE Electron Device Letters, Vol. 17, No. 7, July 1996, Pp. 352-354.	
G	BD	H. Bernhard Pogge, "The Spaces Between the Functions On a Chip", Chemtech, March 1986, Pp. 168-173.	
G	BE	R. Jerome et al., "The Effect of Trench Processing Conditions on Complementary Bipolar Analog Devices with SOI/Trench Isolation", IEEE 1993 Bipolar Circuits and Technology Meeting 3.2, Pp. 41-44.	
	BF		
	BG		
	BH		
	BI		
	BJ		

Examiner Signature	<i>Fourson</i>	Date Considered	8/19/05
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